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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,948	ARIMILLI ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11,13-16 and 18-20* is/are rejected.

7)☒ Claim(s) *6,12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 14 March 2005. Claims 1-20 are pending. New grounds for rejection have been set forth as a result of the instant amendments. Accordingly, this action has been made FINAL.

Claim Rejections - 35 USC § 112

The examiner acknowledges the amendments to the previously rejected claims under 35 U.S.C. 112, second paragraph. In light of these instant amendments along with the remarks given on page 8, paragraph 1, the examiner withdraws the rejections under 35 U.S.C. 112, second paragraph, as given in the previous Office Action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims ~~1-5~~ 1, 3-5, 7-11, 13-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by **Schumann et al. (U.S. Patent No. 5,889,714 hereafter referred to as Schumann)**.

With respect to **independent claim 1,**

"A data processing system, comprising: one or more processing cores; **[FIG. 1, element 12]** *and a memory controller,* **[FIG. 1, element 20]** *coupled to said one or more processing cores,* **[FIG. 1, connecting lines between elements 12 and 20]** *that controls access to a system memory* **[FIG. 1, element 30]** *containing a plurality of rows,* **[Schumann discloses in column 1, lines 60-63, "Second, being synchronous, SDRAM arrays can be split into two or more independent memory banks, and two or more rows can therefore be active simultaneously, with one open row per independent bank."]** *said memory controller having an access history mechanism ~~memory speculation table~~ that ~~stores~~ maintains historical information regarding prior memory accesses,* **[Schumann discloses in the abstract, "The memory controller uses a history register to keep track of the results of a number of prior accesses to each memory bank, remembering whether the access was to the same row as an immediately prior access."]** *wherein said memory controller ~~includes: means~~, responsive to a memory access request, ~~for directing~~ directs an access to a selected row among the plurality of rows in the system memory to service the memory access request;* **[disclosed in the abstract, "For each new memory access, the memory controller either asserts or deasserts a precharge enable signal depending on the state of the**

history bits. As a result, the memory controller is more likely to have a correct row open on a subsequent access..."] *and ~~means for~~ speculatively ~~causing~~ causes the system memory to continue to energize a Row Address Strobe for said selected row following said access* **[Schumann discloses in column 4, lines 28-30, "A row access strobe RAS is used as a signal to activate a selected row of memory cells... A write enable signal WE is used with the CAS signal to select a write operation in the selected memory cell. When CAS is asserted without WE, a memory read operation is performed. When RAS is asserted with WE, a precharge operation is performed."]** *based upon said historical information indicated by said access history mechanism ~~in said memory speculation table~~."* **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30 Schumann further discloses in column 7, lines 31-39, "the history register 246 records the "hit-or-miss" result of the row address comparator 244 for the previous four accesses to the associated bank of SDRAMS 31 under the control of a particular memory bank controller 24. That is, if the access to the bank is to the same row as the previous access, it is recorded as a hit and stored as a logic 1 in the history register 246, whether or not the row was kept open."]**

With respect to independent **claim 8,**

"A memory controller for controlling a system memory of a data processing system, **[FIG. 1, element 20]** *wherein the system memory includes a plurality of rows,* **[Schumann discloses in column 1, lines 60-63, "Second, being**

synchronous, SDRAM arrays can be split into two or more independent memory banks, and two or more rows can therefore be active simultaneously, with one open row per independent bank."] *said memory controller comprising:* ~~*a memory speculation table*~~ *an access history mechanism that* ~~*stores*~~ *maintains historical information regarding prior memory accesses;* **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30]** *and* ~~*means*~~*, a state machine that, responsive to a memory access request,* ~~*for directing*~~ *directs an access to a selected row among the plurality of rows in the system memory to service the memory access request;* **[See FIG. 3 and all associated text within specification, e.g. column 5, lines 30-44. The examiner interprets FIG. 1, element 24 and FIG. 2 as a state machine, outlined in the description in the specification of FIG. 3 "state transition diagram"]** *and* ~~*means for*~~ *speculatively* ~~*causing*~~ *causes the system memory to continue to energize a Row Address Strobe for said selected row* **[Schumann discloses in column 4, lines 28-30, "A row access strobe RAS is used as a signal to activate a selected row of memory cells... A write enable signal WE is used with the CAS signal to select a write operation in the selected memory cell. When CAS is asserted without WE, a memory read operation is performed. When RAS is asserted with WE, a precharge operation is performed."]** *following said access based upon said historical information indicated by said access history mechanism* ~~*memory speculation table*~~*."* **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30]**

With respect to **independent claim 13**,

"A method of operating a memory controller **[FIG. 1, element 20]** *of a system memory of a data processing system, wherein the system memory contains a plurality of rows,* **[Schumann discloses in column 1, lines 60-63, "Second, being synchronous, SDRAM arrays can be split into two or more independent memory banks, and two or more rows can therefore be active simultaneously, with one open row per independent bank."]** *said method comprising: said memory controller ~~storing~~ maintaining historical information regarding prior memory accesses with an access history mechanism ~~in a memory speculation table~~;* **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30]** *in response to receipt of a memory access request, directing an access to a selected row among the plurality of rows in the system memory to service the memory access request;* **[disclosed in the abstract, "For each new memory access, the memory controller either asserts or deasserts a precharge enable signal depending on the state of the history bits. As a result, the memory controller is more likely to have a correct row open on a subsequent access..."]** *and speculatively directing the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism ~~in said memory speculation table~~."* **[Schumann discloses in column 4, lines 28-30, "A row access strobe RAS is used as a signal to activate a selected row of memory cells... A write enable signal WE is used with the CAS signal to select a write operation in the selected memory cell.**

When CAS is asserted without WE, a memory read operation is performed.

When RAS is asserted with WE, a precharge operation is performed."]

With respect to **claims 3, 9, and 14,**

"The data processing system of claim 1, wherein said access history mechanism ~~memory speculation table stores~~ maintains a respective memory access history **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30]** *for each of a plurality of threads executing within said one or more processing cores."* **[FIG. 1, element 12]**

With respect to **claims 4, 10, and 15,**

"The data processing system of claim 1, wherein said plurality of rows in said system memory are arranged in a plurality of banks, **[Schumann discloses in column 1, lines 60-63, "Second, being synchronous, SDRAM arrays can be split into two or more independent memory banks, and two or more rows can therefore be active simultaneously, with one open row per independent bank."]** *and wherein said ~~memory speculation table~~ access history mechanism stores said historical information on a per-bank basis."* **[Schumann discloses in column 7, lines 31-39, "the history register 246 records the "hit-or-miss" result of the row address comparator 244 for the previous four accesses to the associated bank of SDRAMS 31 under the control of a particular memory bank controller 24. That is, if the access to the bank is to the same row as the previous access, it is recorded as a hit and stored as a logic 1 in the history register 246, whether or not the row was kept open."]**

With respect to **claims 5, 11 and 16,**

"The data processing system of claim 1, wherein said plurality of rows are organized in one or more banks, **[Schumann discloses in column 1, lines 60-63]** *and wherein said ~~means for~~ memory controller speculatively ~~continuing~~ continues to energize said Row Address Strobe for said selected row* **[Schumann discloses in column 4, lines 28-30]** *~~comprises means for speculatively continuing to energize said selected row~~ until a next access to another row within a same bank as said selected row."* **[disclosed, e.g. in column 2, lines 47-56 and column 5, lines 1-10]**

[Note: see rejection of claim 8 with respect to claim 11]

With respect to **claim 7,**

"The data processing system of claim 1, wherein said plurality of rows are organized in one or more banks, **[Schumann discloses in column 1, lines 60-63, "Second, being synchronous, SDRAM arrays can be split into two or more independent memory banks, and two or more rows can therefore be active simultaneously, with one open row per independent bank."]** *and wherein said data processing system further comprises ~~comprising~~: a system interconnect coupling* **[FIG. 1, connecting lines between elements 12 and 14]** *said plurality of processing cores;* **[FIG. 1, element 12]** *and one or more cache hierarchies* **[FIG. 1, element 14]** *coupled to said plurality of processing cores that cache data from said system memory, wherein said one or more cache memories communicate historical bank access information to said memory controller."* **[Schumann discloses in column 4, lines 15-20, "The memory**

bank controller 24 consists of...a history register 246..." Schumann also teaches in column 3, lines 18-20, "...the processor 12...communicates with cache 14 and main memory 20 and peripheral devices..." Schumann teaches communication of cache and historical bank access information (via history register) via the processor.]

With respect to **claims 18, 19, and 20**,

"The data processing system of Claim 1, wherein said access history mechanism **[FIG.2 element 246, see all associated text within the specification. See column 4, lines 15-30]** *comprises one or more state machines each having a plurality of different states,* **[See FIG. 3 and all associated text within specification, e.g. column 5, lines 30-44. The examiner interprets FIG. 1, element 24 and FIG. 2 as a state machine, outlined in the description in the specification of FIG. 3 "state transition diagram"]** *wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access."* **[See FIG. 3 and all associated text within specification. Schumann discloses in column 7, lines 31-39, "the history register 246 records the "hit-or-miss" result of the row address comparator 244 for the previous four accesses to the associated bank of SDRAMS 31 under the control of a particular memory bank controller 24. That is, if the access to the bank is to the same row as the previous access, it is recorded as a hit and stored as a logic 1 in the history register 246, whether or not the row was kept open."]**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made..

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being obvious over Schumann et al. (U.S. Patent no. 5,889,714) in view of Gharachorloo et al. (US Patent No. 6,697,919 hereafter referred to as Gharachorloo).

With respect to **claim 2**, Schumann teaches "The data processing system of Claim 1" as stated supra.

Schumann, however, does not disclose *expressly* "wherein said memory controller and said one or more processing cores are integrated within the same circuit chip."

Gharachorloo discloses in column 2, lines 10-14, "...the Alpha 21364 aggressively exploits semiconductor technology trends by including a scaled 1 GHz 21264 core, two levels of caches, memory controller, coherence hardware, and network router all on a single die..." See FIG. 1.

Schumann and Gharachorloo are analogous art because they are from the same field of endeavor, that being memory devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a memory controller and one or more processing cores onto the same integrated circuit chip or die.

The *motivation* for doing so would have been obvious based on the teaching of Gharachorloo in column 2, lines 14-17, **"The tight coupling of these modules enables a more efficient and lower latency memory hierarchy that can substantially improve the performance of commercial workloads."**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Schumann and Gharachorloo before him/her to combine Gharachorloo and Schumann for the benefit of having a memory controller and one or more processing cores integrated onto the same circuit chip or die.

Allowable Subject Matter

Claims 6,12 and 17, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy
Patent Examiner
Art unit: 2189

Reginald G. Bragdon
Supervisory Patent Examiner
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